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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/526,394	03/16/00	HOWELL W	BU9-99-175

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EXAMINER	
PAREKH, N	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/15/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/526,394	Howell et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 10, 2001*

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-4, 6-11, 13, and 14* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-4, 6-11, 13, and 14* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 2 recites the limitation "said same material" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker (US Pat. 5399898) in view of Zhao et al (US Pat. 5674787).

4. Regarding claim 1, Rostoker discloses a metallurgical structure in an integrated circuit (IC)/flip chip having underlying circuitry/components within an exterior covering comprising:

- a passivation/insulating layer (255a in Fig. 2c)

- a via/hole (260d in Fig. 2c) through the passivation layer extending to a metal line (266b in Fig. 2c)

- a barrier layer lining the via (262d in Fig. 2c), and

- a metal plug (264d in Fig. 2c) in the via surrounding the barrier layer wherein the metal plug, barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure, and

- solder bump/connector (252d in Fig. 2c) in direct contact with the conductive/metal plug (264d in Fig. 2c) and the bump being on the planar exterior surface

(Fig. 2c; Col. 12, line 14- Col. 13, line 48; Fig. 1-2c; Col. 7-13).

Rostoker fails to specify forming the barrier layer such that the metal plug is above the barrier layer. Zhao et al teach an interconnect structure in an integrated circuit (IC) where a metal/copper plug is above the barrier layer lining (13/16/17 in Fig. 6) the via (Fig. 6; Fig. 1-14; Col. 5, line 45- Col. 9, line 10). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a barrier layer lining a via such that the metal plug is above the barrier layer to achieve improved protection/insulation for the interconnect structure using Zhao et al's barrier protection in Rostoker's structure.

Regarding claim 2, Rostoker fails to specify the metal plug and the line comprising copper. Zhao et al teach using the metal plug (23 in Fig. 6) and the metal line comprising conventional material such as copper (Col. 5, line 22; Col. 7, line 25). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal plug and the metal line comprising copper to achieve improved electrical performance for the interconnect structure using Zhao et al's material in Rostoker's structure.

Regarding claim 3, Rostoker discloses a barrier layer lining comprising silicon oxide (262d in Fig. 2c) but fails to specify the barrier layer comprising one or more layers of Ti, TiN, Ta and TaN. Zhao et al disclose the bottom barrier layer comprising TiN, Ta, TaN, etc. Furthermore, it is conventional in the chip packaging and interconnection technology art to use the materials such as Ti, Cr, Ta, TiN, etc. to improve the resistance against diffusion of impurities and improve adhesion. The admitted prior art (APA) specify using one or more layers of the materials such as Cr, W, Ti, etc. as a barrier layer. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the barrier layer comprising one or more layers of Ti, TiN, Ta and TaN to improve the resistance against diffusion of impurities in Rostoker's structure in view of Zhao et al.

Claim 6 is rejected as explained above for claim 1.

5. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker (US Pat. 5399898) in view of Zhao et al (US Pat. 5674787) and further in view of Chang et al (US Pat. 5048744) and Havemann (US Pat. 6156651).

Regarding claim 4, as explained above for claim 1, Rostoker in view of Zhao et al disclose using the barrier layers to reduce the diffusion of elements and suppress electromigration (Zhao et al: Col. 5, line 15; Col. 8, line 7-50) but fail to specify the barrier layer and plug preventing the diffusion of elements within the solder bump into the metal line. However, the use of barrier layers such as Ti, TiN, Cr, etc. to provide the diffusion barrier against elements/impurities from solder and to improve adhesion, bond strength and reliability of the interconnection/solder joint is well-known in the chip packaging and interconnection technology art (see prior art disclosed by Gardner et al: Col. 1, line 51). Chang et al teach using Cr/Ti barrier layer to improve the diffusion/interaction and enhance conductivity between the solder and the metal such as copper (Col. 7, line 10; Col. 8, line 33; Fig. 8-11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the barrier layer to prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Chang et al's teaching in Zhao et al's structure in view of Rostoker.

Regarding claim 7, Rostoker in view of Zhao et al fail to specify a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug

being in direct contact with the solder ball. Havemann teaches using conventional multilevel structure forming two levels of copper plugs/grooves with TiN barrier layer such that the second barrier layer is above the first metal plug and second metal plug is above the second barrier layer (Fig. 3G; Col. 4, line 55- Col. 5, line 38). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball to further prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Havemann's teaching in Zhao et al's structure in view of Rostoker.

6. Claims 8-10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker (US Pat. 5399898) in view of Zhao et al (US Pat. 5674787).

The combined teachings of Rostoker and Zhao et al apply to claims 8-10 and 13 as explained above for claims 1-3 and 6 respectively.

7. Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker (US Pat. 5399898) in view of Zhao et al (US Pat. 5674787) and further in view of Chang et al (US Pat. 5048744) and Havemann (US Pat. 6156651).

The combined teachings of Zhao et al, Chang et al and Havemann apply to Rostoker for claims 11 and 14 as explained above for claims 4 and 7 respectively.

B. Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US Pat. 5290732) in view of Zhao et al (US Pat. 5674787).

8. Regarding claim 1, Kumar et al disclose a metallurgical structure in an integrated circuit (IC) chip having underlying circuitry/components within an exterior covering comprising:
- a passivation/insulating layer (16b in Fig. 10)
- a via/hole (Fig. 10) through the passivation layer extending to a metal pad/line (14b in Fig. 9)
- a barrier layer lining the via (18b in Fig. 10), and
- a metal plug (40b in Fig. 10) in the via above the barrier layer wherein the metal plug, barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure, and
- solder bump/connector (44 in Fig. 10) in direct contact with the conductive/metal plug (40b in Fig. 10) and the bump being on the planar exterior surface
(Fig. 10; Col. 5, line 23- Col. 6, line 15; Fig. 5-10; Col. 3-12).

Regarding claim 2, Kumar et al fails to specify the metal plug and the line/pad comprising copper. Zhao et al teach using the metal plug (23 in Fig. 6) and the metal line comprising conventional material such as copper (Col. 5, line 22; Col. 7, line 25). Therefore, it would have

been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal plug and the metal line comprising copper to achieve improved electrical performance for the interconnect structure using Zhao et al's material in Kumar et al structure.

Regarding claim 3, Kumar et al disclose a barrier layer lining comprising one or more layers of Ti, TiN, Ta and TaN (Col. 3, line 30- Col. 4, line 11) to provide the diffusion barrier between the bumps and the metal pad/line.

Claim 6 is rejected as explained above for claim 1.

9. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US Pat. 5290732) in view of Zhao et al (US Pat. 5674787) and further in view of Chang et al (US Pat. 5048744) and Havemann (US Pat. 6156651).

Regarding claim 4, as explained above for claim 1, Kumar et al disclose using the barrier layers to reduce the diffusion of elements but fail to specify the barrier layer and plug preventing the diffusion of elements within the solder bump into the metal line. However, the use of barrier layers such as Ti, TiN, Cr, etc. to provide the diffusion barrier against elements/impurities from solder and to improve adhesion, bond strength and reliability of the interconnection/solder joint is well-known in the chip packaging and interconnection technology art (see prior art disclosed

by Gardner et al: Col. 1, line 51). Chang et al teach using Cr/Ti barrier layer to improve the diffusion/interaction and enhance conductivity between the solder and the metal such as copper (Col. 7, line 10; Col. 8, line 33; Fig. 8-11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the barrier layer to prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Chang et al's teaching in Kumar et al's structure.

Regarding claim 7, Kumar et al fail to specify a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball. Havemann teaches using conventional multilevel structure forming two levels of copper plugs/grooves with TiN barrier layer such that the second barrier layer is above the first metal plug and second metal plug is above the second barrier layer (Fig. 3G; Col. 4, line 55- Col. 5, line 38). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball to further prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Havemann's teaching in Kumar et al's structure.

10. Claims 8-10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US Pat. 5290732) in view of Zhao et al (US Pat. 5674787).

The teachings of Kumar et al and Zhao et al apply to claims 8-10 and 13 as explained above for claims 1-3 and 6 respectively.

11. Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US Pat. 5290732) in view of Zhao et al (US Pat. 5674787) and further in view of Chang et al (US Pat. 5048744) and Havemann (US Pat. 6156651).

The combined teachings of Zhao et al, Chang et al and Havemann apply to Kumar et al for claims 11 and 14 as explained above for claims 4 and 7 respectively.

Response to Arguments

12. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

08-02-01

Sara W Crane

Sara Crane
Primary Examiner